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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/677,596 | 10/02/2003 | William R. Eisenstadt | 5853-268 | 8230 |

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| EXAMINER | |
|---|---|
| PARRIES, DRU M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

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|---|---|
| 05/30/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

TH

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/677,596 | EISENSTADT, WILLIAM R. | |
| | Examiner | Art Unit | |
| | Dru M. Parries | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14,17-27 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,17-27 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 1 and 17 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see page 8, filed March 1, 2007, with respect to claim 12 have been fully considered and are persuasive. The objection of claim 12 has been withdrawn.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5-7, 9-11, 17, 19, 21-23 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigaki (6,463,396) and Dias et al. (4,510,584). Nishigaki teaches a plurality of integrated circuits (inside P2) disposed on a circuit board. He also teaches DC/DC converters (34, 40) for receiving a supply voltage (AC) to produce a plurality of output supply voltages (3.3V, +/-5V and +/-12V). He also teaches processing circuitry (211) for receiving at least one of the output supply voltages (Col. 16, lines 14-18) and an analog time-varying input signal (VCC). Nishigaki also teaches producing a modified time-varying output signal (RMTON) to activate the second power supply circuit (P2). Nishigaki produces the modified signal by modifying the frequency of the input signal (VCC). The modified time-varying output signal being coupled to the inputs of the plurality of integrated circuits. He goes on to teach the processing circuitry comprising analog (via SW1-3) and digital circuitry (Col. 1, lines 22-27).

He goes on to teach that the frequency of the time-varying signal is programmable (the user determines/programs the frequency of VCC by controlling when the computer is docked to and removed from the docking station). He also teaches the processing circuitry (211) comprising an input/output buffer (117). (Fig. 3-5; Cols. 15 and 16) Nishigaki fails to teach the type of signal used to send the signal, RMTON. Dias teaches an activation signal being a 5V pulse (Col. 4, lines 19-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute in Dias' activation signal into Nishigaki's invention for RMTON, since Nishigaki was silent as to the type of signal that it is, and Dias teaches a known type of activation signal. Nishigaki also fails to explicitly teach all the output supply voltages being greater than the supply voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to have all the output supply voltages being greater than the supply voltage since it is just a matter of design choice and would be obvious if the supply voltage was extremely low and the necessary voltages to power each integrated circuit was greater than the supply voltage.

5. Claims 2, 8, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigaki (6,463,396) and Dias et al. (4,510,584) as applied to claims 1 and 17 above, and further in view of Goodfellow et al. (2002/0144163). Nishigaki and Dias teach an integrated circuit as described above. Nishigaki also teaches his time-varying input signal (VCC) being a notification signal regarding the state of the system. Nishigaki fails to teach the time-varying input signal comprising a digital signal. Goodfellow teaches a digital notification signal being sent to the controller regarding the state of the system ([0048]). It would have been an obvious matter of design choice to have the time-varying input signal of Nishigaki be a digital signal, since applicant has not disclosed that the signal being digital solves any stated problem or is for

any particular purpose and it appears that the invention would perform equally well with either an analog or digital signal as the notification signal to the processing circuitry of Nishigaki.

6. Claims 4 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigaki (6,463,396) and Dias et al. (4,510,584) as applied to claims 1 and 17 above, and further in view of Nork et al. (6,411,531) and Roohparvar et al. (6,633,494). Nishigaki and Dias teach an integrated circuit as described above. Nishigaki fails to teach the inner workings of the DC/DC converter. Nork teaches a DC/DC converter receiving opposite phase clock signals ($V_{CLK}$ & $V_{CLKB}$ via oscillator 25; Fig. 3A&B). Nork fails to teach the voltage on those (HIGH/LOW) signals. Roohparvar teaches a clock with a HIGH signal that is representative of the supply voltage, and a LOW signal that is representative of ground (Col. 6, lines 26-28). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Roohparvar's HIGH and LOW voltage values into Nork's oscillator, and implement Nork's DC/DC converter into Nishigaki's invention since Nork and Nishigaki were silent on those specific characteristics and Roohparvar and Nork, respectively, teach an instance that is known in the art.

7. Claims 12-14 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigaki (6,463,396) and Dias et al. (4,510,584) as applied to claims 1 and 17 above, and further in view of Maksimovic et al. ("Switched-Capacitor DC-DC Converters for Low-Power On-Chip Applications"). Nishigaki teaches a circuit as described above. He fails to explicitly teach the type of converter used. Maksimovic teaches a switched capacitor based DC/DC converter (Abstract), which provides passive, peripheral elements for providing programmability to the output voltage of the DC/DC converter. It would have been obvious to one of ordinary

skill in the art at the time of the invention to use Maksimovic's switched capacitor based DC/DC converter as the converter in Nishigaki's invention because it allows for greater efficiency in the circuit and it is known to work in the art and Nishigaki was silent as to the type of converter used.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dru M. Parries whose telephone number is (571) 272-8542. The examiner can normally be reached on Monday -Thursday from 9:00am to 6:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached on 571-272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMP

5-23-2007

5/25/07

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